IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Application of:	EISENSTADT	Confirmation No.:	8230
Application No.:	10/677,596	Examiner:	Parries, Dru M.
Date Filed:	October 2, 2003	Art Unit:	2836

For: **INTEGRATED POWER SUPPLY CIRCUIT FOR SIMPLIFIED BOARD DESIGN**

DECLARATION UNDER 37 C.F.R. §1.131
OF WILLIAM R. EISENSTADT

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, William R. Eisenstadt hereby declare:

1. I am a named inventor of the subject matter claimed in the above-captioned application.

2. I have read the Office Action mailed November 1, 2006.

3. I was a professor in the department of Electrical & Computer Engineering at the University of Florida from a period from prior to Jan 30, 2002 to the present.

4. I have been advised that Japanese Patent Application No. 2002-101558 Suzuki in the Office Action of November 1, 2006 is afforded a date as a reference of April 5, 2002.

5. Before April 5, 2002, I conceived of the claimed subject matter regarding an integrated power supply circuit.

6. In particular, as evidence, I provide a copy of an Invention Disclosure I submitted to the Office of Technology Licensing at the University of Florida, dated January 30, 2002 (marked as "EXHIBIT A"). An annex to the Invention Disclosure was submitted on March 18, 2002, as evidenced by my signature on page 12 of "EXHIBIT A".

7. I exercised diligence regarding the present invention at least from April 5, 2002 (the effective filing date of Suzuki) to October 2, 2003 which is the filing date of the present application. The diligence related activities including further testing of circuits according to the invention, as well as attorney activities relating to drafting the present application.

8. In light of the above, I submit that reasonable diligence towards the claimed invention was exercised during the time period from at least as early as April 5, 2002 to October 2, 2003 (filing date of the present application).

9. I further state that all statements made herein are of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 2/23/2007

William R. Eisenstadt
William R. Eisenstadt

IN TESTIMONY WHEREOF, William R. Eisenstadt has hereunto set his hand this 23rd day of February, 2007.

Witness #1

Erlinda Lane
(Print, Type Name of Witness #1)

Witness #2

Janet Holman Sloan
(Print, Type Name of Witness #2)

(WP367654.2)

UF # 10797

CONFIDENTIAL
INVENTION DISCLOSURE

1. Disclosure of Invention

An invention includes any discovery, new and useful process, composition of matter, article of manufacture, know-how, design, model, technological development, biological material, strain, variety, culture of any organism, or portion, modification translation, or extension of these items, and any mark used in connection with these items. Under patent law, this may include drugs, newly discovered, mutated or genetically engineered microorganisms or plants, new or altered forms of plant life, vaccines, cells, tissue and organ cultures, products of recombinant DNA research, hybrid cell cultures, processes involving microorganisms, monoclonal and polyclonal antibodies, engineered proteins, and some computer programs and designs.

A. TITLE: Integrated Voltage Boost Digital and Analog Circuits for the Design of Simplified Electronic Boards
(Brief, but comprehensive, technically accurate, and descriptive)

B. **CONCISE DESCRIPTION OF THE INVENTION**

1. The disclosure should enable someone having knowledge of the field to understand the invention. Include essential elements (features, concepts, or new results of the invention, whichever is most applicable), their relationship to one another, and their mode of operation. Identify the elements that are considered novel.

Most modern digital board designs contain multiple integrated circuits from different vendors. Depending on the technology and the design of these digital ICs, they usually have several supply voltage requirements and produce several output voltages. For example, a digital electronics board can have 5V, 3.3V, 2.0V and 1.0V circuitry. The problem becomes even more difficult when integrated circuits interface with external standards and connectors such as GPIB, serial port, IRDA, parallel port, VMEbus which can require substantial voltages to maintain good noise margins. In addition, peripheral devices such as LCD displays, keyboards, modems, disk drives, etc. are often attached to digital boards and require additional interface voltages.

Designers often try to select parts with the identical supply logic voltages but often this is not possible. Then, you see what is common on electronic boards today.

a) Multiple voltage supplies with independent voltage regulators and passive filter elements on electronic board. Powertraces nets from these voltage supplies consuming area across the board.

b) Extra integrated circuits that act as voltage translating buffers to convert signals from one supply level to another.

Both of the solutions are costly, and circuit area, parts cost, and design complexity.

I propose an invention that circumvents this problem. This invention will look like a "super" electronic part that can run with a low voltage supply but generates much higher signal levels than the supply voltage. The use of such parts will substantially lower the overall board design costs for digital and analog circuits designers in many cases. These parts can also be used to power up additional electronic parts at a higher supply voltage. In addition, the designers greatly simplified since part count is reduced and reliability will be increased.

The key to this invention is the integration of the active part of a small DC to DC converter and a piece of digital logic, for example, a buffer, or an analog circuit, for example an A/D converter. Low-cost external passive elements to the ICs can be added to the board to lower the integration cost and program the voltage and current levels of the IC power dissipation.

Diagram 1 shows how the system can be implemented in any digital IC design.. The diagram 2 shows how the system can be implemented in analog design. (SEE ATTACHED)

Diagram one shows a DC to DC converter supplied by a low voltage. This DC to DC converter is connected to a digital system which includes four sections, and input buffer, a digital logic section, a signal scale up section, and an output buffer. The low-level logic signals are input and to the input buffer of the digital section. Control signals are connected to the digital logic section of the digital system. The signal scaling up section converts the low-level logic signals to high-level signals The output buffer provides current drive so the signals can be provided to the outside world. The DC to DC converter supplies the necessary voltages for all the digital logic sections. Peripheral passive elements (resistors, capacitors, and inductors) which are external to the IC assist in low-cost implementation of the DC to DC converter and give some programmability to this IC

Digital design variations can be added to this basic structure.

i) The level of the output signals can be programmed via the control signals
ii) Higher power converters can be designated to power several nearby integrated circuits.
iii) Complex digital logic functions, systems and memory and can be added to the digital section of the chip.

2. If the invention is an apparatus or system, attach drawings or a sketch and indicate if it has ever been built or tested. Use additional pages, attach drawings, manuscripts, papers, or other supporting material to facilitate understanding the invention. Attach any data which shows that the invention works.

C. **PRACTICAL FEATURES**: In lay terms, please describe the practical features of the invention.

In most systems, there are all types of chips with different I/O voltages facing each other. This adds a lot of work to the design board. This invention is a small voltage boost circuit internal to an IC that generates additional power, and can shrink the board size (less real estate). This makes the IC more area efficient and less heat is generated if used properly.

D. **PRODUCTS:** Describe the most likely products, services or commercial processes or other applications that could result from this invention (especially important if the invention is a chemical compound).

Digital products with multiple supply voltages, energy efficient products and products with legacy interface standards, RS232, GPIB, VMEbus, etc. Logic family of off-the-shelf products and ASICs will benefit. Analog products and motor interface chips to boost up the voltage output.

E. **BENEFITS**: Describe the primary benefits to a potential customer or user for any products, services, or commercial processes that might be developed from this technology (*e.g.*, what could it do to help a potential customer: lower expenses, increase productivity, efficiency or accuracy, minimize risk, simplify a process, overcome a defect, increase revenue, promote safety?).

It would make their system more efficient and less heat would be generated. It could shrink the board size and require less work for the design board.

F. **What is the stage of development? This invention is at the conceptual stage.**

_x_ Will require prototype simulation.

___ Working prototype
___ Proof of concept
___ Analytical work

What work remains to complete development?

Approximately one year or less.

2. Market Information

Please provide this information to the best of your knowledge We realize this information may not be readily known, but your input will be helpful.

A. **Market Need**

1. What is the ideal market for this technology? Who needs it?

Digital and analog board designers and manufacturers.

2. Why do you think the market needs this technology?

To reduce real estate, minimize heat and lower cost of parts and manufacture.

B. Market Demand

1. What factors influence demand in the market?

Design of new products in market place

2. Is demand becoming weaker or stronger?

Stronger - There will always be a market for this technology as long as there are multiple supply voltages required in board designs

C. Market Size

1. What is the estimated size of the market in annual dollars?

Hundreds of millions of dollars.

2. How did you derive this figure? Please attach any supporting data.

Personal knowledge and expertise in this field.

D. Market Research Information

1. Please list any published technical material such as patents, commercial literature, or scientific articles relating to the invention and any planned future publications.

None

2. Have you conducted any market research? If so, please list your sources.

No

E. Competing Products

1. What existing commercial products or services would this invention directly displace?

None known.

2. What are the competing alternatives or substitutes?

None known.

F. New Developments and Circumvention

1. Are you aware of any new developments (*e.g.*, technologies, products) by others to accomplish the same objective?

None known.

2. How would you "get around" your own invention?

I would have to develop a different design with added interface parts and multiple voltage supplies.

G. Suppliers

1. What companies are the major suppliers for products or services that could or will compete with the invention?

National Semiconductor, AMD, Intersil, Motorola, Texas Instruments, etc. A product line of buffers could be developed that could interface with low voltage microprocessors. Military systems, medical, space and aeronautic systems would benefit.

2. Are there many suppliers or is the market dominated by few companies?

See 1.G

3. Would any of these suppliers be potential licensees?

Yes

H. Competitive Advantages

1. In comparison to currently existing products, services or processes, describe how the subject invention will provide or contribute to superior advantages or benefits.

Reduction in design time, material costs, and assembly. More reliable.

I. Regulatory Issues

1. What are the regulatory or other entry barriers or impediments to the market?

None

3. Potential Licensees/Partners

A. If you are aware of a ***definitive*** licensee or a research sponsor who will license this invention, we must know immediately. Please indicate that company (with specific individual and phone number) in the space below:

_____

_____

B. Where would this invention have the most commercial value? Please indicate your evaluation by ranking the following geographic areas (1 being the highest).

United States	x	Japan	x
Europe	x	Other (Please specify)	x

C. 1. Have you communicated with any industry representative regarding your invention?
YES _____ NO __x__ If yes, please provide the following information:

Date of Disclosure	_____
Company	_____
Address	_____
City/State/Zip	_____
Telephone Number	_____
Individual Contact	_____
Official Title	_____

2. Was such a disclosure made under a confidentiality agreement? YES ____ NO __x__

3. If yes to C.2, please provide a copy of that agreement.

D. Do you wish to license this invention for your own company? YES __x__ NO ____.

Do you wish to discuss this possibility with OTL?

Yes

E. Do you wish to continue research on this invention if the entity licensing the invention provides funding? YES __X__ NO _____

Or self fund

4. Public Disclosure/Publication Plans

Public disclosure includes abstracts and presentations at scientific meetings (including poster sessions), public seminars, shelving of theses, publications, disclosure to others outside of the University who have not signed a confidentiality agreement, and the use, sale, or offer of sale of the invention. Identify dates and circumstances of any such disclosures. Also, indicate your future disclosure or publication plans, and NOTIFY the Office of Technology Licensing (address given in section 9) if the invention becomes publicly disclosed or published in the future (whether by plan or inadvertently)

A. Which of the following have you done or do you intend to do?

		YES	NO	DATE
1.	Publish	____	X	_____
2.	Oral Presentation	____	X	_____
3.	Poster Session	____	X	_____
4.	Disclose to Industry Rep.	____	X	_____
5.	Other Public Dissemination	____	X	_____

5. Financial Support/Contract Identification

The primary purpose of this section is to identify any specific grant or contract number(s) (not the account number) and the external sponsors (governmental agencies, industrial sponsors, private agencies, or others) which provided support used to defray costs related to the research from which the invention resulted. This information is needed to determine whether this invention is subject to any commitments or restrictions arising from the terms of sponsorship. **(NOTE: The percentages indicated in B through E below must add up to 100%.)**

A. Name and address of the University facility, including any Agricultural Research and Development Center, where the invention was developed:

Name	Department of Electrical and Computer Engineering
Address	Post Office Box 116130, University of Florida
City, State, Zip	Gainesville, FL 32611

B. Please provide the following information regarding any contract and grant support of the invention process. (The following information must be provided for EACH contract or grant that supported the invention process; attach additional sheets if necessary.)

Name	_____
Grant/Contract #	_____
Address	_____
City, State, Zip	_____
P.I. Name	_____
Grant/Contract Title	_____

What is the estimated the percentage of contribution through this contract/grant? __0__ %

C. Please provide the following information regarding any support for the invention process by the Florida Agricultural Experiment Station (FAES):

1. List Experiment Station (CRIS) Projects by number and title in effect during the research and development process:

USDA/CSRESS/FLA_____

2. What is the estimated percentage of contribution through the FAES? _____%

D. What is the University's estimated percentage of other support beyond any contracts, grants and/or support by FAES to the invention process? Support includes facilities, personnel, (including yourself) and supplies as well as money in the form of department, University, or gift funds. ___100%

E. What is the estimated percentage of other support? _____%
Please explain the circumstances of this support. (An example would be a co-contributor's independent funding from his or her institution.)

F. Did any of the contributors use any instrument(s) biological, chemical or physical material(s) or substance(s) obtained from others to create this invention? YES _____ NO __X____

If YES, did a Materials Transfer Agreement or other document accompany the transfer?
YES _____ NO _____ Please list any such agreements.

G. Did you or any of the co-contributors submit any University of Florida Disclosure of Outside Activities and Financial Interests, Reporting July 2001- June 2002, Form # OAA-GA-L267-Rev 3/98 for this year or the previous academic year?
YES __X___ NO _____

(If YES, please provide copies of the approved University of Florida Disclosure of Outside Activities and Financial Interests, Form # OAA-GA-L267-Rev. 3/98, with this invention disclosure form.)

Contact our ECE employment office under Linda Brown, 392-9819 for the form copy.

H. Did any of the contributors have academic appointments or employment contracts with institutions other than the University of Florida during the course of this work? If yes, where?

NO

Diagram 1:

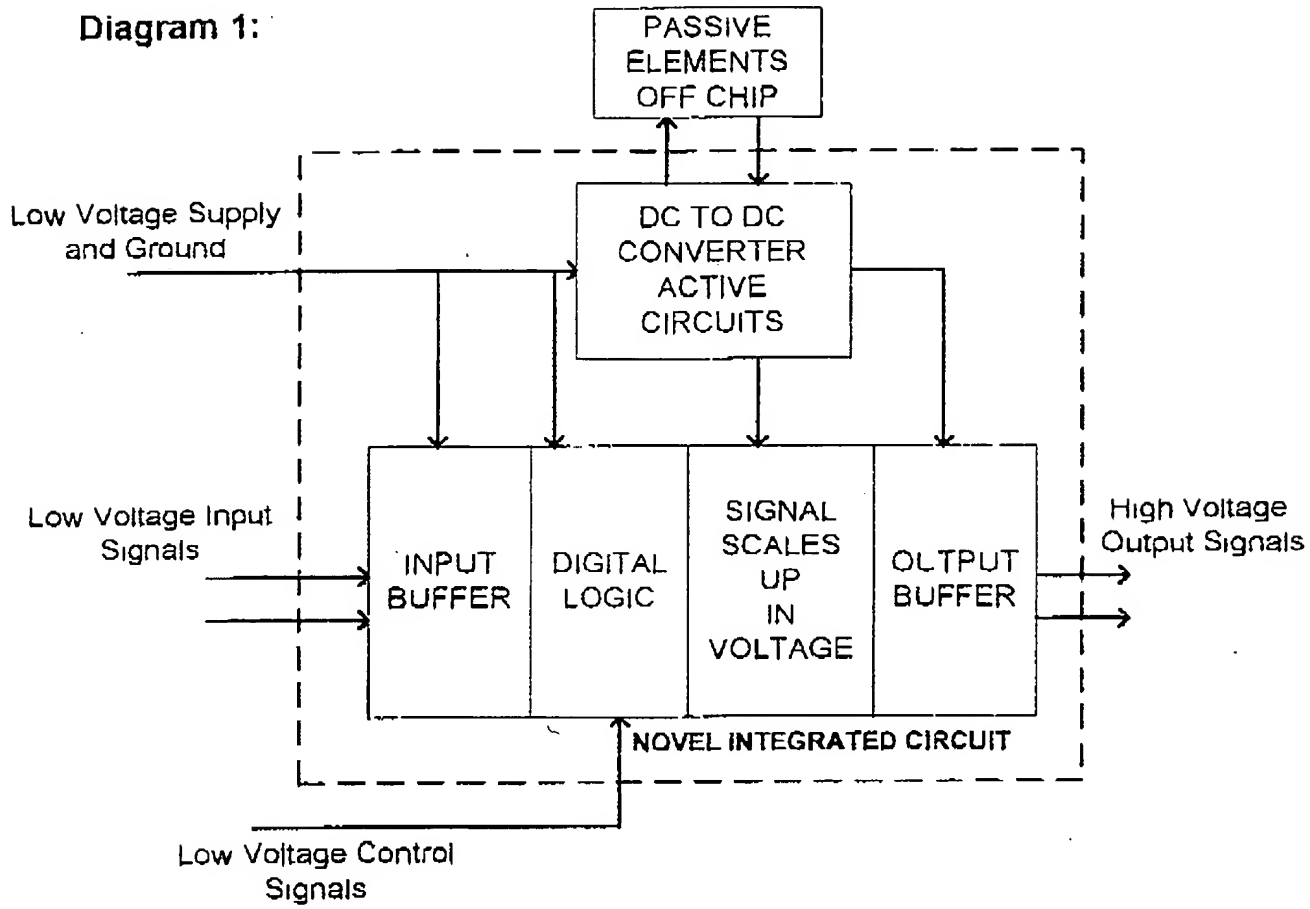
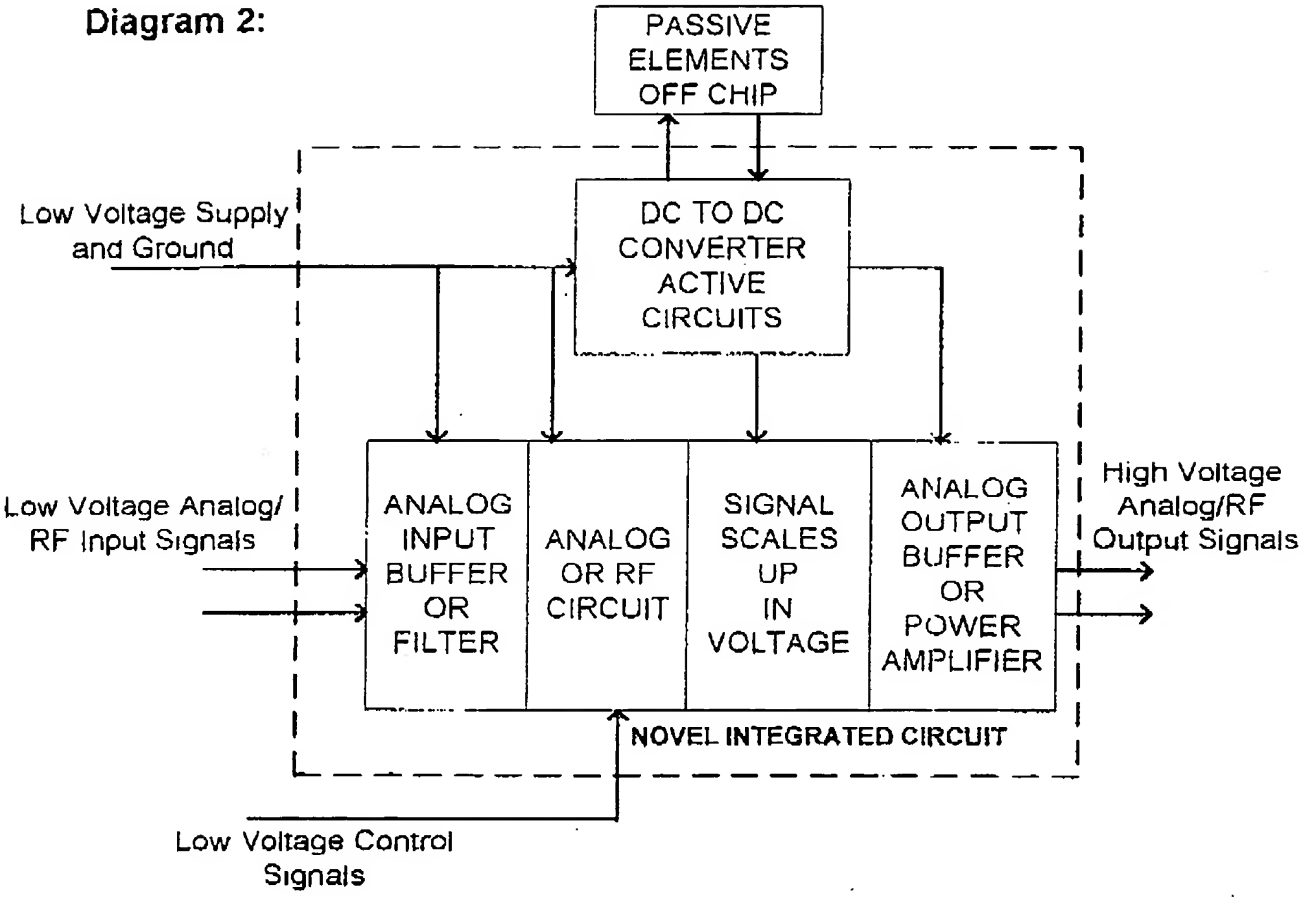

PASSIVE ELEMENTS OFF CHIP
DC TO DC CONVERTER ACTIVE CIRCUITS
Low Voltage Supply and Ground
Low Voltage Input Signals
INPUT BUFFER
DIGITAL LOGIC
SIGNAL SCALES UP IN VOLTAGE
OUTPUT BUFFER
High Voltage Output Signals
NOVEL INTEGRATED CIRCUIT
Low Voltage Control Signals

Diagram 2:


PASSIVE ELEMENTS OFF CHIP
DC TO DC CONVERTER ACTIVE CIRCUITS
Low Voltage Supply and Ground
Low Voltage Analog/ RF Input Signals
ANALOG INPUT BUFFER OR FILTER
ANALOG OR RF CIRCUIT
SIGNAL SCALES UP IN VOLTAGE
ANALOG OUTPUT BUFFER OR POWER AMPLIFIER
High Voltage Analog/RF Output Signals
NOVEL INTEGRATED CIRCUIT
Low Voltage Control Signals

6. Identification of Contributor(s)

List below all persons who are believed to have contributed to the conception or reduction to practice of this invention. Please provide addresses and phone numbers where they may be contacted. Please make additional copies of this page if necessary.

Researcher # 1

First Name: **William** Middle Name: **R.** Last Name: **Eisenstadt**

529 33 Electrical & Computer Engineering Post Office Box 116130 CAMPUS	4315 NW 75th ST
Work Address	Home Address
Gainesville, FL 32611-6130 USA	Gainesville, FL 32606
City, State, Zip, Country	City, State, Zip, Country
(352) 392-4946	(352) 371-2273
Work Phone Number	Home Phone Number
(352) 392-8382	wrc@tec.ufl.edu
Work Fax Number	e-mail Address
271-74-3404	US
Social Security Number	Citizenship

Electrical and Computer Engineering

Researcher title and University affiliation, e.g., Department, Center, College

Researcher # 2

First Name	Middle Name	Last Name
Work Address		Home Address
City, State, Zip, Country		City, State, Zip, Country
Work Phone Number		Home Phone Number
Work Fax Number		e-mail Address
Social Security Number		Citizenship

Researcher title and University affiliation, e.g., Department, Center, College

Note: The foregoing list should include names of all persons who may qualify as legal inventors. Inventorship is a legal question, which is generally determined by the attorney of record at the time a patent application is filed. A statement, which discusses the concept of inventorship, is available from the Office of Technology Licensing.

7. Signatures

Signature of researcher submitting disclosure:

William R. Eisenstadt
William R. Eisenstadt

William R. Eisenstadt
Signature

3/18/02
Date

8. Distribution

Send the original and one copy of the completed disclosure to the Office of Technology Licensing, 317 Walker Hall, P.O. Box 115500, Gainesville, FL 32611, Telephone: (352) 392-8929.

EXHIBIT "B"

UNIVERSITY OF FLORIDA

Research and Graduate Programs
Office of Technology Licensing

PO Box 115500
Gainesville, FL 32611-5500
(352) 392-8929
Fax: (352) 392-6600
http://www.otl.ufl.edu

March 28, 2002

BY FACSIMILE
(561) 653-5333

Greg Nelson, Esquire
AKERMAN SENTERFITT
222 Lakeview Avenue, Suite 400
West Palm Beach, Florida 33401-6147

Re: Invention Disclosure entitled "*Integrated Voltage Boost Digital and Analog Circuits for the Design of Simplified Electronic Boards)*"
UF#- 10797
Inventors: William R. Eisenstadt

Dear Mr. Nelson:

Please proceed with the preparation of a provisional patent application on the above-referenced technology as soon as possible. Should you require additional information to allow you to prepare a thorough patent application, please feel free to contact the inventors to obtain the needed information, or contact our office for any assistance needed to accomplish this.

We have assigned UF#-10797 to this case. Please reference this UF# on all correspondence regarding this case. All correspondence regarding this case should be addressed to me and copied to all inventors, when appropriate.

If you have any questions regarding these instructions, please give me a call or contact me by email. My email address is ammarder@ufl.edu telephone (352) 846-1512. You may reach my licensing associate, Sheila Johndrow, at 392-8961 or by email johndrow@ufl.edu.

Sincerely,

Alan M. Marder
Assistant Director

cc: Dr. William R. Eisenstadt

EXHIBIT

Neil R. Jetter - RE: 10797

From: "Sheila Johndrow" <johndrow@ufl.edu>
To: "Neil R. Jetter" <NJetter@Akerman.com>
Date: 6/19/2002 7:25 AM
Subject: RE: 10797

Sorry for the incorrect date. That was the date we first authorized another law firm to prepare the application, and I just used that same letter, forgetting to change the date. I will print it out again with the correct date. The date that you were authorized is correct in our database and in our file (and probably on the fax cover sheet) I will resend it if you wish. sheila

-----Original Message-----
From: Neil R. Jetter [mailto:NJetter@Akerman.com]
Sent: Tuesday, June 18, 2002 5:14 PM
To: johndrow@ufl.edu
Subject: 10797

Dear Sheila,

I noticed the letter to Greg Nelson from Al Marder authorizing our work on this case (which we received on June 6, 2002) was dated March 28, 2002.
If possible, we would appreciate a corrected date for the authorizing letter.

best regards,
Neil Jetter

From the desk of
Neil R. Jetter
Akerman, Senterfitt & Eidson, P.A.
222 Lakeview Avenue, Ste. 400
West Palm Beach, Florida 33401
Direct 561-671-3662
Telefax 561-653-5333
e-mail: njetter@akerman.com

UNIVERSITY OF FLORIDA

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http://www.otl.ufl.edu

May 31, 2002

Gregory Nelson, Esquire
AKERMAN SENTERFITT
222 Lakeview Avenue, Suite 400
West Palm Beach, Florida 33401-6147

Re: Invention Disclosure entitled *"Integrated Voltage Boost Digital and Analog Circuits for the Design of Simplified Electronic Boards)"*
UF#- 10797
Inventors: William R. Eisenstadt

Dear Mr. Nelson:

Please proceed with the preparation of a provisional patent application on the above-referenced technology as soon as possible. Should you require additional information to allow you to prepare a thorough patent application, please feel free to contact the inventors to obtain the needed information, or contact our office for any assistance needed to accomplish this.

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If you have any questions regarding these instructions, please give me a call or contact me by email. My email address is ammarder@ufl.edu telephone (352) 846-1512. You may reach my licensing associate, Sheila Johndrow, at 392-8961 or by email johndrow@ufl.edu.

Sincerely,

Alan M. Marder
Assistant Director

cc: Dr. William R. Eisenstadt